Hardware Design Engineer

About Vsora :

VSORA is a French fabless semiconductor company delivering ultra-high-performance AI inference solutions for both data centers and edge deployments. Our proprietary architecture achieves exceptional implementation efficiency, ultra-low latency, and minimal power draw - dramatically cutting inference costs across any workload. Fully programmable and agnostic to both algorithms and host processors, our chips serve as versatile companion platforms. A rich instruction set lets them seamlessly handle pure AI, pure DSP, or any hybrid of the two, all without burdening developers with extra complexity. To streamline development and shorten time-to-market, VSORA embraces industry standards: our toolchain is built on LLVM and supports common frameworks like ONNX and PyTorch, minimizing integration effort and customer cost. Based in the outskirts of Paris, France, the company was founded in 2015 by a team of highly qualified and accomplished AI/DSP experts and entrepreneurs.

Job Summary:

We are seeking a Hardware Design Engineer to lead end-to-end development of high-performance electronic boards hosting VSORA AI accelerator chipset following the OCP Open Accelerator Infrastructure (OAI) standard. The purpose is to design and build several electronic boards (OAM, UBB and intermediate test boards), as reference designs, to be integrated in a high performance compute server. This role owns the complete hardware lifecycle from architecture, schematic design through PCB layout, simulation, board bring-up and debug. The ideal candidate is hands-on, detail-oriented, and experienced with high-speed and high-power accelerator platforms.

Key Responsibilities:

- Define the electronic boards architecture, in particular the power management structure and components able to deliver high current to the AI accelerator IC with the expected PDN performances in DC and AC.
- Realize the schematics, pre layout simulations and select all needed components.
- Drive PCB layout execution (outsourced), including definition of constraints, review of the high-speed signals routing, power/ground plane strategy, PCB stack-up definition and the technical communication with PCB/PCBA suppliers.

- Execute and/or drive Power Integrity (PI) simulation to verify IR Drop, impedance profiles and ensure overall PDN performance can meet the design specifications.
- Perform Signal Integrity (SI) simulation to verify high speed signals (PCIe Gen5) performances.
- Setup the lab to be able to execute the board bringup, debug and electronic validation.

Requirements and skills:

- Master's degree in electrical engineering or related field
- 3-5 years of relevant experience in hardware design and development
- Proven expertise in:
    - Schematic capture and layout oversight of complex PCB designs
    - High density and multiple layers PCB designs (16+ layers)
    - Hands-on experience with board bring-up and lab debug
- Experience in one or more of the following domains is highly appreciated:
    - High-speed signals, such as PCIe Gen5 or equivalent high speed interfaces
    - Power delivery network (PDN) for high-power ASICs or FPGA
    - Signal Integrity (SI) and Power Integrity (PI) analysis using industry-standard tools

Additionally, the following skills can be a plus:

- Familiarity with computer server architectures and solutions
- Experience with AI accelerator or GPU/ASIC platforms
- Familiarity with OCP OAI or OCP server standards

Contact :

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