



Next generation AI inference super-chip partitionning study in TSMC 5nm process

Company presentation :

[VSORA](#) is a French fabless semiconductor company delivering ultra-high-performance AI inference solutions for both data centers and edge deployments. Our proprietary architecture achieves exceptional implementation efficiency, ultra-low latency, and minimal power draw—dramatically cutting inference costs across any workload.

Fully programmable and agnostic to both algorithms and host processors, our chips serve as versatile companion platforms. A rich instruction set lets them seamlessly handle pure AI, pure DSP, or any hybrid of the two, all without burdening developers with extra complexity.

To streamline development and shorten time-to-market, VSORA embraces industry standards: our toolchain is built on LLVM and supports common frameworks like ONNX and PyTorch, minimizing integration effort and customer cost.

After the tape-out of Horus chip (TSMC 5nm process) in the Jotunn SIP (from 2 to 8 chip per package), in October 2025, the next iteration of the chip is already on the way and requires evaluating how to split the design in a relevant way to achieve better quality of result and lower runtimes.

Skills (mandatory, nice to have):

- Languages : **System Verilog**, *SystemC*, **Python**, **Tcl**, *bash*, *C++*, *cmake*
- **STA basics** (**setup-hold**, **recovery-removal**, *Clock-domain crossing*, ...)
- **DFT basics** (*stuck at tests*, *test at speed*, **memory bist**, ...)
- *Low power* (*level-shifting*, *power switching*, *isolation*, *UPF-1801 standard*, ...)
- *Physical implementation basics* (*floorplanning*, *placement constraints*, *CTS concepts*, ...)

Internship content

Length : 6 months

Tasks :

- 1) Hands on with the implementation flow of an existing subblock <1M instances (*1-2 months*)
 - a) Synthesis

- b) DFT insertion
- c) Floorplan, Placement and CTS
- 2) Partitionning study of a macro block (> 5M instances) (*4 -5 months*)
 - a) Study design architecture of the macro-block
 - b) Propose partitionning strategies
 - c) Study impacts on the following flow steps
- 3) Extending study on other macro blocks (*optionnal*)
- 4) Report redaction (*0,5 month dedicated*)

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